U.S.S.N. 09/588,788

Claim Amendments

Please amend claims 1, 4, and 19 as follows:

Listing of Claims

1. (currently amended) A method for fabricating an integrated circuit planar inductor with an enhanced Q value comprising:

providing a substrate comprising a dielectric layer over a semiconductor substrate;

forming over the substrate a planar spiral conductor layer comprising a single spiral to form a planar spiral inductor, wherein a successive series of loops within the planar spiral conductor layer is formed with a progressive and discontinuous variation, said variation progressing from a center of said spiral defined by a first loop to a periphery of said series of loops at least one of:

a series of progressive stepwise changes in linewidths to form a series of discrete linewidths for the successive series of loops; and

a series of progressive stepwise changes in spacings separating the successive series of loops;

wherein said center of said spiral defined by said first loop surrounds a planar surface of said dielectric layer to define an inner cavity.

Claims 2-3 (cancelled)

4. (currently amended) A method for fabricating an integrated circuit planar inductor with an enhanced Q value comprising:

providing a substrate comprising a dielectric layer over a semiconductor substrate;

forming on the substrate a planar spiral conductor layer to form a planar spiral inductor, wherein a successive series of loops within the planar spiral conductor layer is formed with a progressive and discontinuous variation, said variation progressing in any direction from a center of said spiral defined by a first loop to a periphery of said series of loops, said variation comprising at least one of:

a series of progressive stepwise changes in linewidths to form a series of discrete linewidths for the successive series of loops; and

a series of progressive stepwise changes in spacings separating the successive series of loops;

wherein the successive series of loops is formed in a shape selected from the group consisting of a triangle, a square, a rectangle, a higher order polygon, a uniform ellipse and a circle, wherein said center of said spiral defined by said first loop ~~consists of~~ surrounds a planar surface of said dielectric layer to define an inner cavity.

5. (original) The method of claim 1 wherein the planar spiral conductor layer is formed of a conductor material selected from the group consisting of non-magnetic metal, non-magnetic metal alloy, magnetic metal, magnetic metal alloy, doped polysilicon and polycide conductor materials, and laminates thereof.

6. (previously presented) The method of claim 1 wherein the progressive stepwise changes to form a series of discrete linewidths increases from the first loop which defines the center of the planar spiral inductor having a comparatively narrow linewidth to a final loop which defines the perimeter of the planar spiral inductor having a comparatively wide linewidth.

7. (original) The method of claim 6 wherein the comparatively narrow linewidth is from about 7 to about 10 microns and the comparatively wide line width is from about 17 to about 21 microns.

8. (previously presented) The method of claim 1 wherein the successive series of loops comprising the single spiral comprises from about 1 to about 8 loops.

Claims 9-15 (cancelled)

16. (previously presented) The method of claim 1 wherein the progressive and discontinuous variation comprises progressively increasing or decreasing stepwise changes.

17. (previously presented) The method of claim 1, wherein the successive series of loops is formed in a shape selected from the group consisting of a triangle, a square, a rectangle, a higher order polygon, a uniform ellipse and a circle.

18. (previously presented) The method of claim 4 wherein the progressive stepwise changes to form a series of discrete linewidths increases from a first loop which defines the center of the planar spiral inductor having a comparatively narrow linewidth to a final loop which defines the perimeter of the planar spiral inductor having a comparatively wide linewidth.

19. (currently amended) A method for fabricating an integrated circuit planar inductor with an enhanced Q value comprising:

providing a substrate comprising a dielectric layer over a semiconductor substrate;

forming over the substrate a planar spiral conductor layer comprising a single spiral to form a planar spiral inductor, wherein a successive series of loops within the planar spiral conductor layer is formed with a progressive and discontinuous variation, said variation progressing in any direction from a center of said spiral defined by a first loop to a periphery of said series of loops, said variation comprising a series of progressive stepwise changes in spacings separating the successive series of loops;

wherein said center of said spiral defined by said first loop surrounds a planar surface of said dielectric layer to define an inner cavity.

20. (previously presented) The method of claim 19 wherein said variation further comprises a series of progressive stepwise changes in linewidths to form a series of discrete linewidths for the successive series of loops.

21. (previously presented) The method of claim 20 wherein the progressive stepwise changes to form a series of discrete linewidths increases from a first loop which defines the center of the planar spiral inductor having a comparatively narrow linewidth to a final loop which defines the perimeter of the planar spiral inductor having a comparatively wide linewidth.

22. (previously presented) The method of claim 19, wherein the progressive and discontinuous variation comprises progressively increasing or decreasing stepwise changes.

23. (cancelled)

24. (previously presented) The method of claim 1, wherein the

successive series of loops is formed in a shape selected from the group consisting of a triangle, a square, a rectangle, and a higher order polygon.